Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (original) A semiconductor device, comprising:

a semiconductor substrate;

a nonvolatile memory cell that includes

a memory transistor realized by a MOS transistor including a memory gate oxide film that is arranged on the semiconductor substrate, and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state; and

a selection transistor realized by a MOS transistor that is serially connected to the memory transistor, the selection transistor including a selection gate oxide film that is arranged on the semiconductor substrate, and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film;

wherein the memory gate oxide film is arranged to be thinner than the peripheral circuit gate oxide film.

2. (original) The semiconductor device as claimed in claim 1,

wherein the memory transistor and the selection transistor are PMOS

transistors.

3. (original) The semiconductor device as claimed in claim 1,

wherein the selection gate oxide film and the memory gate oxide film are arranged to have a same thickness.

4. (original) The semiconductor device as claimed in claim 1,

wherein the selection gate oxide film and the peripheral circuit gate oxide film are arranged to have a same thickness.

5. (original) The semiconductor device as claimed in claim 1, further comprising:

a capacitor including a lower electrode made of polysilicon that is arranged on the semiconductor substrate via an insulating film, and an upper electrode made of polysilicon that is arranged on the lower electrode via a capacitor insulating film;

wherein the floating gate and the lower electrode are created from a same polysilicon layer, and the capacitor insulating film is arranged on an upper surface and a side surface of the floating gate.

6. (original) The semiconductor device as claimed in claim 5,

wherein the peripheral circuit gate and the upper electrode are created from a same polysilicon layer.

7. (original) The semiconductor device as claimed in claim 5,

wherein the selection gate, the floating gate, and the lower electrode are created from the same polysilicon layer.

8. (original) The semiconductor device as claimed in claim 6,

wherein the selection gate, the peripheral circuit gate, and the upper electrode are created from the same polysilicon layer.

9. (currently amended) A semiconductor device, comprising:

a divider resistor circuit that is configured to obtain a voltage output through voltage division and adjust the voltage output through cutting one or more fuse elements;

the divider resistor circuit including

a plurality of resistance value adjusting resistor elements ~~the~~ that are serially connected;

a plurality of fuse MOS transistors as the fuse elements that are connected in parallel to the resistance value adjusting resistor elements;

a nonvolatile memory cell that includes a memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a memory gate oxide film that is arranged on a semiconductor substrate and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is

arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film which peripheral circuit gate oxide film is arranged to be thicker than the memory gate oxide film.

10. (currently amended) A semiconductor device comprising:

a voltage detecting circuit that includes a divider resistor circuit that divides an input voltage and outputs the divided voltage, a reference voltage generating circuit that generates a reference voltage, and a comparator circuit that compares the divided voltage from the divider resistor circuit with the reference voltage from the reference voltage generating circuit;

the divider resistor circuit including

a plurality of resistance value adjusting resistor elements ~~the~~ that are serially connected;

a plurality of fuse MOS transistors as the fuse elements that are connected in parallel to the resistance value adjusting resistor elements;

a nonvolatile memory cell that includes a memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a

memory gate oxide film that is arranged on a semiconductor substrate and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film which peripheral circuit gate oxide film is arranged to be thicker than the memory gate oxide film.

11. (currently amended) A semiconductor device comprising:

a constant voltage generating circuit that includes an output driver that controls output of an input voltage, a divider resistor circuit that divides an output voltage and outputs the divided voltage, a reference voltage generating circuit that generates a reference voltage, and a comparator circuit that compares the divided voltage from the divider resistor circuit with the reference voltage from the reference voltage generating circuit and controls an operation of the output driver according to the comparison result;

the divider resistor circuit including

a plurality of resistance value adjusting resistor elements ~~the~~ that are serially connected;

a plurality of fuse MOS transistors as the fuse elements that are connected in parallel to the resistance value adjusting resistor elements;

a nonvolatile memory cell that includes a memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a memory gate oxide film that is arranged on a semiconductor substrate and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film which peripheral circuit gate oxide film is arranged to be thicker than the memory gate oxide film.

12. (original) A semiconductor device comprising:

a semiconductor substrate;

a nonvolatile memory cell that includes

a memory transistor realized by a MOS transistor including a memory gate oxide film that is arranged on the semiconductor substrate, and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state; and

a selection transistor realized by a MOS transistor that is serially connected to the memory transistor, the selection transistor including a selection gate oxide film that is arranged on the semiconductor substrate, and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film;

wherein an impurity concentration within the polysilicon of the floating gate is arranged to be lower than an impurity concentration within the polysilicon of the peripheral circuit gate oxide film.

13. (original) The semiconductor device as claimed in claim 12,

wherein an impurity concentration within the polysilicon of the selection gate is equal to the impurity concentration within the polysilicon of the floating gate.

14. (original) The semiconductor device as claimed in claim 12,

wherein an impurity concentration within the polysilicon of the selection gate

is equal to the impurity concentration within the polysilicon of the peripheral circuit gate.

15. (original) The semiconductor device as claimed in claim 12,

wherein the memory gate oxide film, the selection gate oxide film, and the peripheral circuit gate oxide film are arranged to have a same thickness.

16. (original) The semiconductor device as claimed in claim 12,

wherein the memory gate oxide film is arranged to be thinner than the peripheral circuit gate oxide film.

17. (original) The semiconductor device as claimed in claim 16,

wherein the selection gate oxide film and the memory gate oxide film are arranged to have a same thickness.

18. (original) The semiconductor device as claimed in claim 16,

wherein the selection gate oxide film and the peripheral circuit gate oxide film are arranged to have a same thickness.

19. (original) The semiconductor device as claimed in claim 12,

wherein the memory transistor and the selection transistor are PMOS transistors.

20. (currently amended) A semiconductor device, comprising:

a divider resistor circuit that is configured to obtain a voltage output through voltage division and adjust the voltage output through cutting one or more fuse elements;

the divider resistor circuit including

a plurality of resistance value adjusting resistor elements ~~the~~ that are serially connected;

a plurality of fuse MOS transistors as the fuse elements that are connected in parallel to the resistance value adjusting resistor elements;

a nonvolatile memory cell that includes a memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a memory gate oxide film that is arranged on a semiconductor substrate and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film, the polysilicon of the peripheral circuit gate being arranged to have an impurity concentration that is higher than an impurity concentration within the polysilicon of the

floating gate.

21. (currently amended) A semiconductor device comprising:

a voltage detecting circuit that includes a divider resistor circuit that divides an input voltage and outputs the divided voltage, a reference voltage generating circuit that generates a reference voltage, and a comparator circuit that compares the divided voltage from the divider resistor circuit with the reference voltage from the reference voltage generating circuit;

the divider resistor circuit including

a plurality of resistance value adjusting resistor elements ~~the~~ that are serially connected;

a plurality of fuse MOS transistors as the fuse elements that are connected in parallel to the resistance value adjusting resistor elements;

a nonvolatile memory cell that includes a memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a memory gate oxide film that is arranged on a semiconductor substrate and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film, the polysilicon of the peripheral circuit gate being arranged to have an impurity concentration that is higher than an impurity concentration within the polysilicon of the floating gate.

22. (currently amended) A semiconductor device comprising:

a constant voltage generating circuit that includes an output driver that controls output of an input voltage, a divider resistor circuit that divides an output voltage and outputs the divided voltage, a reference voltage generating circuit that generates a reference voltage, and a comparator circuit that compares the divided voltage from the divider resistor circuit with the reference voltage from the reference voltage generating circuit and controls an operation of the output driver according to the comparison result;

the divider resistor circuit including

a plurality of resistance value adjusting resistor elements ~~the~~ that are serially connected;

a plurality of fuse MOS transistors as the fuse elements that are connected in parallel to the resistance value adjusting resistor elements;

a nonvolatile memory cell that includes a memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a memory gate oxide film that is arranged on a semiconductor substrate and a floating gate

made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film, the polysilicon of the peripheral circuit gate being arranged to have an impurity concentration that is higher than an impurity concentration within the polysilicon of the floating gate.